UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/531,397	03/21/2000	Joseph C. Ballantyne	3797.81466	6866

28319 7590 12/23/2004

BANNER & WITCOFF LTD.,
ATTORNEYS FOR MICROSOFT
1001 G STREET , N.W.
ELEVENTH STREET
WASHINGTON, DC 20001-4597

EXAMINER	
ALI, SYED J	

ART UNIT	PAPER NUMBER
2127	

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/531,397	BALLANTYNE, JOSEPH C.	
	Examiner	Art Unit	
	Syed J Ali	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,13-19,21-25,27-30 and 34-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,13-19,21-25,27-30 and 34-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 13, 2004 has been entered.

2. This office action is in response to the amendment filed October 13, 2004. Claims 1-8, 13-19, 21-25, 27-30, and 34-38 are presented for examination.

3. The text of those sections of Title 35, U.S. code not included in this office action can be found in a prior office action.

Claim Rejections - 35 USC § 103

4. **Claims 1-8, 13-19, 21-25, 27-30, and 34-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gee et al. (USPN 6,374,286) (hereinafter Gee).**

5. As per claim 1, Gee teaches the invention as claimed, including a method of scheduling CPU resources comprising the steps of:

using a counter to determine when to allocate the CPU resources (col. 23 lines 19-29);

instructing an interrupt controller, via non-maskable interrupts from the counter, to allocate the CPU resources (col. 23 lines 40-55; col. 25 lines 13-23); and

instructing the CPU to allocate resources in real-time by the interrupt controller issuing non-maskable interrupts to the CPU (col. 25 line 30 - col. 26 line 17).

6. It is noted that Gee specifically refers to the interrupt controller as an input/output controller (IOC), and uses other terminology that is not explicitly equivalent to the terms used in the claimed invention. However, Gee uses the same methodology of utilizing non-maskable interrupts to perform context switching as claimed. A programmable counter counts clock ticks and/or machine cycles to determine when to issue a non-maskable interrupt signaling the CPU to switch from execution of one JVM thread to another. The use of a non-maskable interrupts allows the JVM to execute at a highest priority and prevents it from being preempted before its time slice finishes.

7. As per claims 2-5, Gee teaches the invention as claimed, including allocating either a portion or all of the CPU resources (col. 3 lines 22-35; col. 23 lines 19-29) to at least one thread (col. 20 lines 53-55; col. 23 lines 33-40) by determining a duration of time and a periodicity for execution of said at least one thread (col. 23 lines 24-29; col. 23 lines 40-43; col. 24 lines 23-27).

8. As per claims 13-16, 19, 34, 36-37 Gee teaches the invention as claimed, including a method of scheduling resources on at least one microprocessor that includes at least one performance counter (col. 28 lines 45-54; col. 29 lines 41-50) or timer (col. 23 lines 19-29), at least one programmable interrupt controller (col. 23 lines 40-55), and at least one CPU (col. 8 line 59 - col. 9 line 3), the method comprising the steps of:

allowing the CPU to execute a first thread (col. 25 lines 26-29);

issuing a first non-maskable interrupt from the performance counter or timer to the programmable interrupt controller upon determining on a real-time basis that it is time to allocate the resources to a second thread (col. 23 lines 19-29);

instructing the programmable interrupt controller to issue a second non-maskable interrupt to the CPU that instructs the CPU to perform a context switch (col. 25 lines 19-29);

instructing the CPU to stop execution of the first thread (col. 25 lines 30-33);

causing the CPU to store first current state information regarding execution of the first thread (col. 25 lines 33-37) and restore current state information regarding execution of the second thread (col. 25 lines 56-65), wherein state information is made up of stack data, processor data, and floating point-unit data (col. 20 lines 30-57);

setting the counter to specify when the counter will turn over again (col. 23 lines 24-43); and

allocating resources to the second thread (col. 25 line 66 - col. 26 line 17).

9. As per claims 6-8 and 21-22, Gee teaches the invention as claimed, including the counter being a performance counter that counts machine cycles or executed computer instructions in order to determine when to allocate the CPU resources (col. 28 lines 45-54; col. 29 lines 41-50).

10. As per claims 17-18 and 35, Gee teaches the invention as claimed, including the programmable interrupt controller being an APIC (col. 23 lines 44-55) and the microprocessor being selected from the group consisting of a Pentium 4GB, a Pentium Pro 64GB, a Pentium MMX 4GBN MMS, a Pentium II 4GB MMX, a Pentium III 4GB MMS KNI, a Celeron 4GB

MMX, a Xeon PII 64GB MMX and a Xeon PIII 64GB MMX KNI (col. 7 line 66 - col. 8 line 5; col. 8 line 47 - col. 9 line 3).

11. As per claims 23-25, Gee teaches the invention as claimed, including instructions for executing said at least one thread at a highest IRQ level (col. 22 lines 45-51) in a transparent manner so that at least one operating system process is unaware of the execution of said at least one thread (col. 23 lines 19-43) as a single real-time thread (col. 23 lines 30-43; col. 33 lines 47-53).

12. As per claims 27-30, Gee teaches the invention as claimed, including allocating at least a portion of a CPU's resources to an operating system process (col. 24 lines 37-43) and using the remaining CPU resources for execution of said at least one thread (col.24 lines 8-36), and releasing the CPU resources back to the operating system process or to another thread when said at least one thread finishes execution (col. 23 lines 30-43) at the expiration of a predetermined number of CPU cycles for execution allocated for execution between the operating system process and said at least one thread (col. 23 lines 24-29; col. 24 lines 23-27).

13. As per claim 38, Gee teaches the invention as claimed, including the second execution thread being executed after interrupts, which were pending when the interrupt service routine finished (col. 23 lines 52-55), have been executed and after deferred procedure calls (col. 23 lines 30-33), which were pending when the interrupt service routine finished executing, have been executed (col. 23 line 67 - col. 24 line 13).

Response to Arguments

14. Applicant's arguments with respect to claims 1-8, 13-19, 21-25, 27-30, and 34-38 have been considered but are moot in view of the new grounds of rejection.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed J Ali whose telephone number is (571) 272-3769. The examiner can normally be reached on Mon-Fri 8-5:30, 2nd Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai T An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Syed Ali
December 13, 2004

MENG-AI T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100